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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chason et al.

Serial No.: 10/044,777

Filed: January 11, 2002

Title: SEMICONDUCTOR RACKAGE
DEVICE AND METHOD

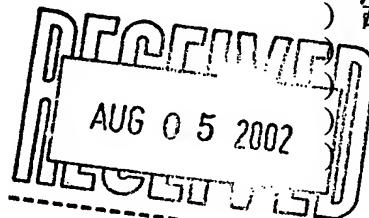
Group Art
Unit: 2811

Examiner: Jones, J.

CERTIFICATE OF MAILING

I hereby certify that this paper is
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1/17/02 Kelly Bressel



INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Dear Sir:

This Information Disclosure Statement is being submitted in accordance with 37
C.F.R. §§1.97 - 1.98 in connection with the above-identified application. The following
documents are listed below.

U.S. Patent Documents

Patent No.	Inventor(s)	Issue Date
6,395,124	Oxman et al.	5/28/02
6,376,278	Egawa et al.	4/23/02
6,352,881	Nguyen et al.	3/5/02
6,352,878	Mostafazadeh et al.	3/5/02
6,335,571	Capote et al.	1/1/02
6,341,418	Brouillette et al.	1/29/02

6,323,062	Gilleo et al.	11/27/01
6,297,560	Capote et al.	10/2/01
6,287,893	Elenius et al.	9/11/01
6,245,595	Nguyen et al.	6/12/01
6,238,223	Cobbley et al.	5/29/01
6,194,788	Gilleo et al.	2/27/01
6,171,887	Yamaji	1/9/01
6,168,972	Wang et al.	1/02/01
6,132,646	Zhou et al.	10/17/00
6,121,689	Capote et al.	9/19/00
6,075,290	Schaefer et al.	6/13/00
6,017,634	Capote et al.	1/25/00
5,985,456	Zhou et al.	11/16/99
5,985,043	Zhou et al.	11/16/99
5,956,605	Akram et al.	9/21/99
5,925,936	Yamaji	7/20/99
5,814,401	Gamota et al.	9/29/98
5,128,746	Pennisi et al.	7/7/92

U.S. Published Applications

Publication No.	Publication Date	Inventor(s)
US 2001/0012680 A1	August 9, 2001	Cobbley et al.
US 2002/0014703 A1	February 7, 2002	Capote et al.

Foreign Patent Documents

Document No.	Country	Publication Date
WO 99/03597	PCT	1/28/99
WO 99/04430	PCT	1/28/99
WO 99/56312	PCT	11/4/99
WO 00/54322	PCT	9/14/00
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Other References

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Mr. Albert Capote et al., "A Novel Flip-Scale package Using Pre-Applied Multilayer Flip-Chip Under-Encapsulation," Pan Pacific Microelectronics Symposium pg. 153-158 (1999)

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Nadia Yala et al., "Characterization of Flip Chip Assembly Utilizing Wafer Applied Underfill," ECTC, 5 pages (2002)

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Q. Tong et al., "Encapsulant Materials and Processes for Wafer Level-Chip Scale Packaging (WL-CSP)," IEEE, 7 pages (2002)

Robert V. Burress et al., "A Novel, Wafer-Scale Technology for Addressing Process and Cost Obstacles Associated with Underfilling FCOB," IEEE, 4 pages (2002)

The above items are listed on Form PTO-SB-08A which accompanies this Information Disclosure Statement. A copy of each document cited thereon is enclosed herewith.

Pursuant to 37 CFR §1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b).

The Commissioner is hereby authorized to charge any additional fees which may be required in this application to Deposit Account No. 06-1135.

Respectfully submitted,
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